

# GainSight: A Unified Framework for Data Lifetime Profiling and Heterogeneous Memory Composition

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## ABSTRACT

As AI workloads drive increasing memory requirements, domain-specific accelerators need higher-density on-chip memory beyond what current SRAM scaling trends can provide. Simultaneously, the vast amounts of short-lived data in these workloads make SRAM overprovisioned in retention capability. To address this mismatch, we propose a wholesale shift from uniform SRAM arrays to heterogeneous on-chip memory, incorporating denser short-term RAM (StRAM) devices whose limited retention times align with transient data lifetimes.

To facilitate this shift, we introduce GainSight, the first comprehensive, open-source framework that aligns dynamic, fine-grained workload lifetime profiles with memory device characteristics to enable generation of optimal StRAM memory compositions. GainSight combines retargetable profiling backends with an architecture-agnostic analytical frontend. The various backends capture cycle-accurate data lifetimes, while the frontend correlates workload patterns with StRAM retention properties to generate optimal memory compositions and project performance.

GainSight elevates data lifetime to a first-class design consideration for next-generation AI accelerators, enabling systematic exploitation of data transience for improved on-chip memory density and efficiency. Applying GainSight to MLPerf Inference and PolyBench workloads reveals that 64.3% of first-level GPU cache accesses and 79.01% of systolic array scratchpad accesses exhibit sub-microsecond lifetimes suitable for high-density StRAM, with optimal heterogeneous on-chip memory compositions achieving up to 3× active energy and 4× area reductions compared to uniform SRAM hierarchies.

To facilitate adoption and further research, GainSight is open-sourced at <https://gainsight.stanford.edu/>.

## KEYWORDS

Heterogeneous on-chip memory, profiling, domain-specific accelerators, AI/ML workloads

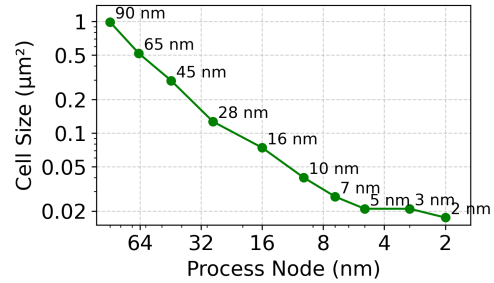


Figure 1: Scaling trend of 6T SRAM, revealing a stagnating trajectory [50, 53].

## 1 INTRODUCTION

The rapid growth of data-intensive AI workloads drives demand for greater memory capacity in domain-specific accelerators to optimize locality and energy efficiency. Large language models (LLMs) exemplify this demand, with parameter size scaling by almost 400× every two years while accelerator memory capacity only doubles in that same span [12]. This widening gap exacerbates the proverbial *memory wall*, where insufficient on-chip memory capacity creates performance bottlenecks and forces costly off-chip memory accesses [2].

The conventional approach of increasing on-chip SRAM capacity faces significant scaling limitations, as shown in Figure 1. On-chip SRAM scaling has plateaued at 0.021 µm<sup>2</sup> per cell across 5 nm to 3 nm process nodes [53]. Even the latest gate-all-around (GAA) 2nm transistor process struggles to restore earlier scaling trajectories [50], as maintaining the delicate variation control between transistor sizing and threshold voltages becomes increasingly difficult at smaller geometries and lower operating voltages [18]. This scaling challenge creates a critical perf/mm<sup>2</sup> bottleneck for accelerator design as integrating more SRAM on reticle-limited dies reduces the available area for logic, forcing difficult trade-offs between compute and on-chip memory resources.

At the same time, data lifetime – empirically defined as the duration that a data structure is retained in memory before it is no longer needed – is highly heterogeneous within and across workloads and hardware architectures. This exposes a core design tension: *while existing memory systems offer consistent and uniform data retention capabilities, real-world data usage patterns require widely different lifetime durations.*

Specifically, data short-livedness is increasingly pervasive in modern AI workloads. AI analytic pipelines commonly write, quickly ingest, and then discard or overwrite gigabytes of information. To list only three examples in LLM inference: (1) the decoding process commonly generates multiple candidate output tokens only to retain one; (2) massive attention score matrices exist just long enough for softmax computation before invalidation; (3) particularly in high-throughput auto-regressive LLM inference, the *key* and *value* activation matrices, known as the KV cache, monopolize GPU HBM and are temporarily moved on-chip into SRAM before immediate consumption by the tensor cores. We can back-calculate that many of these generated data structures persist for mere microseconds in modern hardware accelerators or GPUs.

These large amounts of highly transient data represent an architectural opportunity: rather than store them in SRAM, which dominates on-chip area, they can be stored in higher-density, short-retention memory technologies.

Given these trends, conventional memory can evolve from a uniform address space of random access memory to a heterogeneous collection of denser short-term and long-term memories with varying retention properties that match application-specific traffic patterns and lifetime requirements [30]. This transformation mirrors the evolution from general-purpose CPUs to domain-specific accelerators in the computing space, where specialization around workload characteristics enabled greater performance and efficiency. Just as compute has specialized, so too must memory.

Table 1 presents various memory technologies for on-chip integration, with a particular focus on short-term RAM (StRAM) devices<sup>1</sup> that directly address the data transience challenge. StRAM devices like gain cell RAM (GCRAM) and embedded DRAM (eDRAM) provide 2-4× higher density and significantly lower leakage power than SRAM for transient data, despite μs-scale retention times [5, 14, 19, 27, 28]. The key insight is that these retention constraints become advantages rather than limitations when data lifetimes are shorter than device retention times, enabling refresh-free operation with superior density and lower energy consumption.

We therefore reimagine on-chip memory through differentiated compositions of GCRAM, eDRAM, and SRAM that exploit data transience to outperform traditional SRAM-centric designs. Realizing these gains requires treating data lifetime as a first-class design constraint and developing systematic methodologies and tools to correlate lifetime patterns with memory device retention properties.

However, existing accelerator design workflows and workload profiling tools are insufficient for providing this level of insight. Prior methodologies for designing memory arrays with StRAM devices [8, 44] relied on static dataflow heuristics without profiling of

<sup>1</sup>The term “device” in this paper refers to memory cells of a particular memory technology (e.g., SRAM, GCRAM); this should not be confused with system-level I/O “devices” such as GPUs, network cards, etc.

**Table 1: Comparison of on-chip memory technologies: from traditional SRAM to short-term RAM (StRAM) offering higher density and lower read/write active energies by trading off retention time. Long-term RAM (LtRAM) options are also included for completeness.**

	SRAM	Long-term RAM	Short-term RAM
<b>Structure</b>	6T SRAM	MRAM, RRAM, FeRAM, etc.	2T/3T GCRAM, 1T1C eDRAM
<b>Benefits</b>	Long retention & balanced R/W perf.	Dense, 3D-stackable, long retention, low read energy	Dense, 3D-stackable, low leakage power
<b>Drawbacks</b>	Area scaling issues, high static power	Expensive writes, limited endurance	Short retention, expensive refreshes
<b>Uses</b>	Fast read and write caching	Rarely written, static data cache	Fast write-then-read ops. for dynamic data

transient lifetime patterns, rendering them less extensible to workloads exhibiting complex dynamic memory access patterns. Existing profilers [34, 36, 55] provide coarse-grained performance counters that fail to capture the fine-grained, cycle-accurate data lifetime dynamics necessary for StRAM evaluation. Their architecture-specific implementations also prevent systematic analysis across various accelerator backends beyond CPUs and GPUs [41].

These deficiencies leave critical questions about accelerator workloads and prospective memory architectures unanswered:

- How long do data objects persist in on-chip memory across different workloads and architectures?
- How do lifetime patterns correlate with StRAM retention limits to minimize refresh overhead?
- Given a library of StRAM devices, how can we compose them in an on-chip memory array to create an optimal mix that minimizes area and active energy consumption?

To address these research questions, we introduce *GainSight*, the first comprehensive framework for lifetime-aware heterogeneous on-chip memory design that establishes data lifetime as a systematic design discipline. Unlike existing profilers that provide narrow, platform-specific cache statistics, GainSight pioneers a unified methodology that bridges dynamic workload lifetime patterns with StRAM device characteristics to identify refresh-free operation opportunities. This work makes three synergistic contributions to lifetime-aware on-chip memory design:

- **Profile-Guided Heterogeneous Memory Composition:** We establish the first systematic approach for automatically generating optimal heterogeneous on-chip memory compositions based on dynamic workload data lifetimes and memory access patterns. This transforms memory design from intuition-driven to profile-guided optimization that exploits workload transience, providing actionable guidelines for accelerator design.
- **Unified Profiling and Evaluation Framework:** We implement GainSight through retargetable accelerator backends capturing fine-grained memory access traces across various accelerator architectures, coupled with an architecture-agnostic analytical frontend supporting multiple memory

Table 2: Comparison of on-chip memory runtime profilers

Profiler	GPU Profiling	Accelerator Profiling	Profile Kernels	Profile Cache Lines	Profile Byte Accesses	Correlate with Mem. Device	Auto Mem. Array Composition	Open-Source
MemSpy [31]	✗	✗	✓	✓	✗	✗	✗	✗
CacheGrind [42]	✗	✗	✗	✓	✗	✗	✗	✓
perf mem [26]	✗	✗	✓	✓	✓	✗	✗	✓
DProf [36]	✗	✗	✓	✗	✗	✗	✗	✓
Nsight Compute [33]	✓	✗	✓	✗	✗	✗	✗	✗
rocProfiler [1]	✓	✗	✓	✗	✗	✗	✗	✓
GMPProf [55]	✓	✗	✓	✓	✗	✗	✗	✓
GainSight (Ours)	✓	✓	✓	✓	✓	✓	✓	✓

device evaluations. This infrastructure systematically correlates processing architectures, StRAM devices, and workloads to inform heterogeneous memory composition.

- **Cross-Platform Case Studies:** We demonstrate GainSight’s versatility through evaluations across GPU and systolic array architectures (Section 6), analyzing MLPerf Inference and PolyBench workloads to provide concrete provisioning guidelines. Our studies reveal that optimal heterogeneous compositions achieve up to 3× active energy and 4× area reductions compared to uniform SRAM.

To facilitate adoption and further research, GainSight’s source code is available at <https://code.stanford.edu/tambe-lab/gainsight>, with comprehensive documentation and interactive visualizations at <https://gainsight.stanford.edu/>, enabling the broader community to explore lifetime-aware on-chip memory design principles.

## 2 BACKGROUND AND RELATED WORKS

While prior work has explored non-SRAM on-chip memory architectures and various forms of memory profiling tools, their varied scopes and limitations mean that no single methodology systematically connects fine-grained workload data lifetime profiles with the design process of memory systems in accelerators. This section establishes the technical foundation for GainSight’s methodology, covering non-SRAM short-term memory technologies, existing on-chip memory profiling and design approaches, and the data lifetime concept that enables heterogeneous memory composition.

### 2.1 Short-Term RAM Devices

Given SRAM’s scaling limitations and the transient nature of AI workload data, alternative short-term memory (StRAM) technologies have been designed to offer superior density and energy efficiency by trading off retention time for area and energy benefits. Figure 2 shows the circuit topologies of the memory devices evaluated in GainSight: six-transistor (6T) static random-access memory (SRAM), two-transistor (2T) gain cell RAM (GCRAM), and one-transistor-one-capacitor (1T1C) embedded DRAM (eDRAM).

**SRAM**, as the conventional on-chip memory device technology, provides fast access and indefinite retention through cross-coupled inverters but faces scaling limitations and overprovisioning for  $\mu$ s-scale AI data lifetimes.

**Gain Cell RAM (GCRAM)** uses 2-3 transistors per cell and utilizes the read transistor as a transconductance amplifier to convert

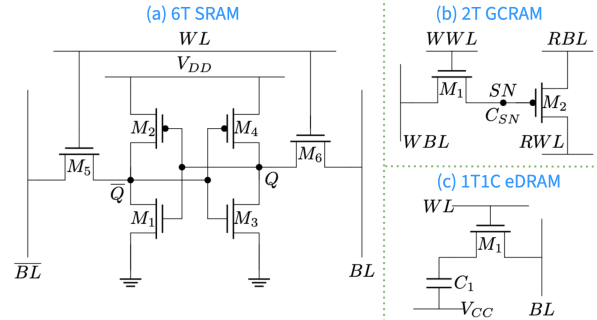


Figure 2: Circuit diagrams of 6T SRAM, 2T GCRAM, and 1T1C eDRAM. Note the smaller transistor count of GCRAM and eDRAM vs. SRAM. To further save area, the write transistor  $M_1$  of GCRAM and the capacitor  $C_1$  of eDRAM can be 3D stacked on top of silicon at backend-of-line [9, 29] – optimization opportunities unavailable to SRAM.

the stored voltage into an amplified bitline current for read sensing, achieving 2-4× higher density and lower leakage than SRAM [5]. Comprised of silicon transistors fabricated with conventional fin field-effect (FinFET) processes, **Si-GCRAM** offers  $\mu$ s-scale retention with SRAM-comparable latencies [14, 35].

**Hybrid-GCRAM** replaces the write nMOS transistor in Si-GCRAM ( $M_1$  in Figure 2(b)) with an oxide semiconductor transistor made of materials such as indium tin oxide (ITO) through back-end-of-line (BEOL) manufacturing processes. This design achieves longer retention compared to Si-GCRAM and higher density through 3D stacking of the ITO transistor on top of silicon peripheral circuits [7, 29]. However, there is an inverse tradeoff between its retention and write frequency [27], necessitating even closer examination of workload memory access patterns to avoid refresh overhead.

Traditionally, it has been challenging to integrate dynamic RAM (DRAM) into on-chip memory architectures due to capacitor fabrication complexities. However, recently proposed **embedded DRAM (eDRAM)** designs enable on-chip integration using oxide transistors and BEOL processes, providing ms-scale retention with high density [9] but higher active energy than GCRAM due to charge-sharing read mechanisms.

**Table 3: Architectures leveraging non-SRAM short- or long-term on-chip memory devices**

Name	Target Workload	Memory Type	Memory Device
DaDianNao [8]	CNN inference	Short-term	eDRAM
RANA [44]	CNN inference	Short-term	eDRAM
CAMEL [54]	CNN/Transformer training	Short-term	GCRAM
STT-AI Ultra [32]	CNN training/inference	Long-term	MRAM
CHIMERA [13]	CNN training	Long-term	RRAM

These technologies offer distinct retention-energy-area tradeoffs that GainSight can correlate with workload lifetime patterns to identify optimal heterogeneous compositions.

## 2.2 Memory Profilers

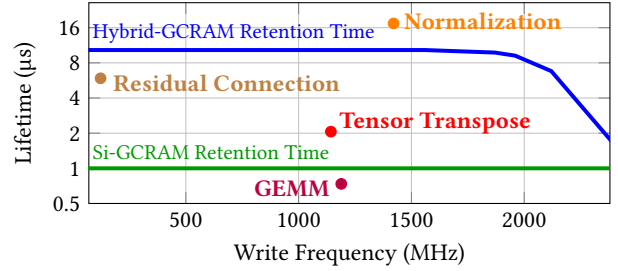
Effectively utilizing StRAM requires understanding fine-grained data lifetimes and memory access patterns through profiling of target workloads to inform on-chip memory system design decisions. While promising in theory, existing approaches exhibit critical limitations that prevent principled exploitation of data transience. Table 2 compares existing profilers with GainSight’s capabilities, highlighting their limitations in coarse granularities and limited architecture scopes. We also observe that existing profilers are primarily retrospective analysis tools without systematic correlation of profiling results to prospective memory device characteristics, as they are not intended as design tools.

CPU profiling is well-established through tools like Linux perf mem [26] and full-system simulators such as MemSpy [31] that track fine-grained memory accesses and cache behavior. DProf [36] correlates sampled cache misses with program structures, identifying inefficiencies in data layout and cache utilization. GPU profilers such as NVIDIA’s Nsight Compute [33] and CUPTI [34] provide only kernel-level granularity and aggregated statistics regarding on-chip cache usage, without characterizing individual memory access behaviors or data lifetime patterns crucial for heterogeneous memory composition. GMProf [55] achieved finer granularity but uses abstract memory constructs that do not map to physical on-chip memory arrays.

## 2.3 Accelerators with Emerging Memories

Various attempts have been made, as summarized in Table 3, to address *Memory Wall* bottlenecks in accelerators by integrating non-SRAM on-chip memory devices as shown in Table 1, including gain cell RAM (GCRAM), embedded DRAM (eDRAM), resistive RAM (RRAM) and magnetoresistive RAM (MRAM).

The common thread in these designs is that they combine conventional processing elements (e.g., SIMD, systolic arrays) with novel memory devices, typically using static heuristics of predictable dataflows in workloads to estimate data lifetimes relative to device retention characteristics. However, these heuristic-based approaches are typically specialized and lack generalization, and must be re-evaluated when newer and emerging models such as state-space models [17] come online.



**Figure 3: Data lifetimes and write frequencies for Llama-3.2-11b operations [15] executed on a GPU backend compared against 5nm Si-GCRAM and Hybrid-GCRAM retention limits [27].**

GainSight bridges the aforementioned research gaps by providing comprehensive fine-grained profiling across arbitrary workloads and hardware backends, as well as the ability to systematically correlate these profiles with StRAM device characteristics to generate optimal heterogeneous memory compositions. This unified approach resolves both profiling granularity limitations and the lack of quantitative design insights in current memory systems. Such systematic design exploration enables next-generation heterogeneous memory architectures that effectively exploit workload data transience.

## 2.4 Data Lifetime Concept

Data lifetime quantifies the time interval during which a data structure incorruptibly lives in memory to satisfy application functional correctness, forming the key metric for correlating workload behavior with retention-constrained memory devices.

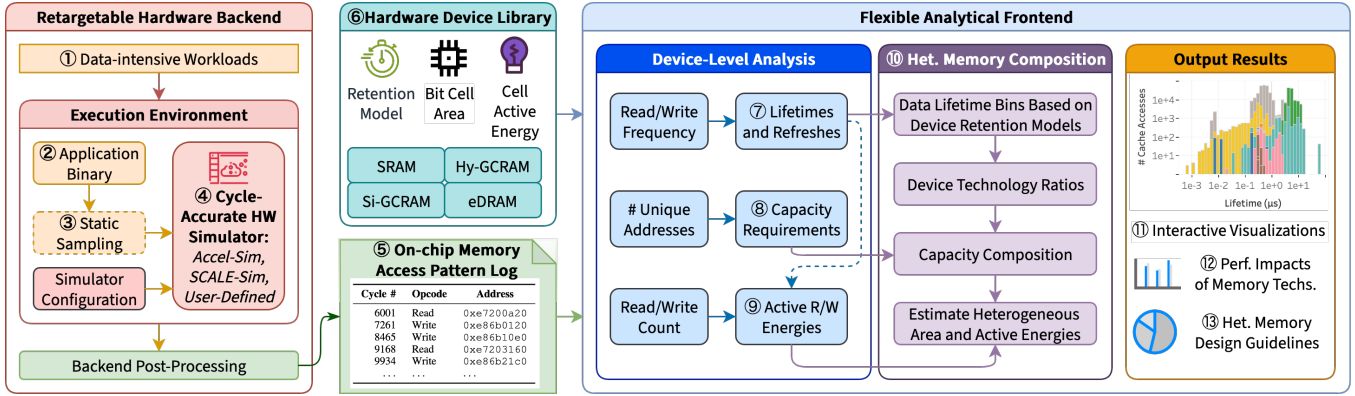
*Definition 2.1.* The **lifetime** of a data structure at a given memory address is the time between its **first write** and **last read** before being overwritten or invalidated.

This definition adapts across memory implementations. Scratchpad lifetimes span from stores to final reads before overwriting, while cache lifetimes extend from stores or misses to the last hit before subsequent misses or stores.

Memory device suitability depends on lifetime-retention correlation. **Short-lived** data with lifetimes below device retention enables refresh-free operation, while **long-lived** data requires refresh mechanisms or longer-retention alternatives.

Figure 3 demonstrates this principle using Llama-3.2-11B H100 kernel lifetimes [15] against Si-GCRAM and Hybrid-GCRAM characteristics, with write frequency effects on GCRAM retention capabilities.

This analysis reveals that GEMM operations exhibit lifetimes compatible with the retention capabilities of Si-GCRAM and tensor operations align with Hybrid-GCRAM, while normalization operations’ lifetimes exceed both memory devices’ retention limits and require eDRAM or SRAM to avoid refresh overhead. These patterns exemplify the foundation for GainSight’s systematic approach to matching data transience with appropriate device technologies in heterogeneous memory compositions to enable refresh-free operation.



**Figure 4: GainSight framework organization, comprising retargetable hardware backends and a flexible analytical frontend. The primary output of the backend is a memory access trace; the frontend inputs this trace, along with specifications of memory device models, to produce performance projections and heterogeneous on-chip memory design guidelines.**

### 3 GAINSIGHT ORGANIZATION

GainSight is designed as a comprehensive framework for analyzing on-chip memory behavior, addressing the question: “What are the tangible benefits of replacing on-chip SRAM with heterogeneous compositions of short-term memory devices for different workloads and hardware backends?”

To answer this, GainSight performs the following key tasks:

- (1) Capture fine-grained on-chip memory access traces for arbitrary workloads on retargetable hardware backends.
- (2) Extract lifetime statistics, read/write frequencies, and capacity utilization patterns.
- (3) Correlate lifetime characteristics with memory device retention properties and other characteristics to project memory array area and active energy metrics.
- (4) Generate optimal heterogeneous compositions of high-density StRAM that minimize energy consumption through refresh-free operation.
- (5) Provide interactive visualizations that inform lifetime-aware design decisions.

To meet these requirements, GainSight comprises two main components: retargetable hardware backends that connect to an architecture-agnostic analytical frontend, as shown in Figure 4. The backends execute workloads on hardware architectural simulators and generate fine-grained, cycle-accurate memory access traces with lifetime annotations. The frontend processes these traces to extract data lifetime statistics, correlates them with retention-limited StRAM characteristics, projects optimal heterogeneous memory compositions, and provides interactive visualizations for design insights. The memory device library includes post-fabrication models of SRAM, Si-GCRAM [14], Hybrid-GCRAM [28], and 1T1C eDRAM [9].

#### 3.1 Usage Scenario

Hardware accelerator designers seeking to exploit data transience can leverage GainSight as a comprehensive design exploration tool that bridges workload analysis with heterogeneous memory provisioning decisions.

The primary input designers provide is a set of representative AI workloads relevant to their target application domain, which can be executed on the provided backends of a SIMD GPU or systolic array accelerator. For specialized prospective architectures not covered by the existing backends, users may optionally implement custom backends as described in Section 4.3.

GainSight generates three complementary output formats that directly inform memory hierarchy design decisions. Quantitative JSON reports provide concrete metrics including refresh requirements, active energy consumption, and area projections for both individual StRAM devices and optimal heterogeneous compositions. Interactive visualizations enable exploration of lifetime distributions and device correlation patterns across workloads and kernel subroutines.

Most critically, the framework produces detailed specifications for optimal heterogeneous memory compositions, including capacity quantities, area allocations, and projected energy benefits compared to uniform SRAM designs.

These outputs provide insights to enable architects to make data-driven provisioning decisions for heterogeneous memory arrays before costly physical prototyping.

The following sections describe GainSight’s retargetable backends and analytical frontend architecture.

### 4 RETARGETABLE HARDWARE BACKEND

GainSight’s retargetable hardware backends execute workloads on a variety of accelerator architectures to capture fine-grained memory access traces and data lifetime statistics. This multi-backend approach is essential because memory access patterns and data lifetimes vary significantly across different hardware architectures, even for identical workloads, due to varying dataflow patterns and on-chip memory organizations.

Since existing runtime profilers lack the granularity required for lifetime-aware analysis as discussed in Section 2.2, we implement simulation-based backends by modifying architectural simulators to generate the fine-grained traces necessary for StRAM device evaluation. Simulation-based approaches enable arbitrary memory

hierarchy configurations and support evaluation of hypothetical compositions that are not yet available in physical hardware, making them essential for design space exploration of emerging memory technologies.

Our implementation includes GPU and systolic array accelerator backends, but GainSight can integrate any backend capable of generating fine-grained traces in the required format ⑤ in Figure 4.

## 4.1 Backend 1: Simulating GPU Architectures

Single instruction, multiple data (SIMD) architectures have become the standard for accelerating deep learning workloads, with NVIDIA GPUs being a leading example. To capture memory access patterns and data lifetime metrics for SIMD architectures, we modified Accel-Sim v1.3.0 [23], a cycle-accurate GPU simulator for use as GainSight’s first backend.

The GPU backend generates traces through a multi-stage process following Figure 4. CUDA-based workloads ① are first processed by an NVBit [47]-based tracing utility to capture SASS assembly code for each kernel ②. The assembly code then undergoes offline kernel clustering and sampling ③ [3] to select representative kernels for simulation, which is necessary due to the high computational cost of cycle-accurate GPU simulation. These representative traces are fed into GPGPU-Sim v4.2.1 [4, 23] to simulate program execution and collect memory access traces at each individual cycle and instruction ④, generating detailed on-chip cache access traces to facilitate lifetime analysis ⑤.

Our modifications to Accel-Sim include logging call insertions at the interfaces between the streaming multiprocessors (SMs) and the L1 and L2 caches to record address, access type, timing, and hit/miss status of each cache operation. We focus on L1 and L2 caches, which are most relevant for AI workloads and offer the greatest optimization opportunities through heterogeneous compositions.

**4.1.1 Simulator Performance and Program Sampling.** The computational overhead of cycle-accurate GPU simulation presents a significant challenge for memory system evaluation, especially for contemporary AI workloads, with Accel-Sim requiring 6-7 orders of magnitude longer execution time than native GPU hardware [46].

To address this simulation speed challenge, we leverage the inherent repetitiveness of deep learning computations, where similar layer structures recur throughout models [20, 39, 45] and identical operations execute across different data batches [6, 21], enabling us to sample representative kernels rather than simulating every single kernel in a workload. We adopt the Principal Kernel Analysis (PKA) methodology [3], a silicon-validated sampling technique that identifies representative kernel subsets through hierarchical clustering based on offline analysis of kernel characteristics.

Table 4 demonstrates the effectiveness of PKA-based sampling across representative AI workloads, showing substantial reductions in simulation requirements while preserving sufficient accuracy for memory system analysis. The sampling process reduces executed kernels to as few as 0.15% of the original workload (LLaMA-3-8B), achieving speedups ranging from 10.89 $\times$  to 412.76 $\times$  across different model architectures. The mean absolute error (MAE) for critical memory metrics remains bounded.

**Table 4: Key figures of merit of kernel sampling applied to selected AI workloads running on the GPU backend, with average baseline lifetimes, write frequencies, Si-GCRAM area requirements, and Si-GCRAM active energies estimated at around 83.5  $\mu$ s, 339 MHz, 11 mm<sup>2</sup> and 23.5 kJ, respectively.**

Workload	Sampled (%)	Speedup ( $\times$ )	Lifetime MAE ( $\mu$ s)	Write Freq MAE (MHz)	Area MAE (mm <sup>2</sup> )	Energy MAE (kJ)
bert-base-uncased	8.37%	10.89	0.36	11.59	0.00	1.09
llama-3-8b	0.15%	412.76	3.76	21.39	0.91	3.65
resnet-50	10.31%	60.97	3.73	10.09	0.00	1.99

This workload sampling approach is extensible to other prospective backends, enabling acceleration of all simulation-based evaluations of GainSight.

## 4.2 Backend 2: Simulating Systolic Arrays

For systolic array-based accelerators, we extend the open-source SCALE-Sim [41], a Python-based simulator for convolution or GEMM-based DNN networks. SCALE-Sim models three peripheral SRAM buffers – input (*ifmap*), weight (*filter*), and output (*ofmap*) – and provides the essential features for our backend implementation: cycle-accurate simulations, configurable buffer sizes, adjustable computation dataflow, processing element array dimensions, and built-in memory access trace generation.

Following Figure 4, the backend starts from target workload specifications ① and extracts binary forms of model hyperparameters and GEMM operands ② executable on the cycle-accurate simulator ④. The simulator’s key tunable parameters include processing element array dimensions and dataflow configuration, with SCALE-Sim supporting input-stationary, weight-stationary, or output-stationary modes that determine how data streams through processing elements and buffers.

## 4.3 Bring Your Own (Hardware) Backend

Beyond the GPU and systolic array implementations, GainSight’s architecture enables integration of arbitrary hardware backends capable of generating fine-grained memory access traces. The analytical frontend processes any backend-generated traces that adhere to the standardized format shown in ⑤ of Figure 4. This format includes detailed timestamps, address ranges, and read/write types for each memory access. This extensibility allows hardware simulators or physical accelerators to serve as alternative backends, provided they can generate the required trace granularity and support compilation of target workloads ① into executable binary code ②.

Architectural differentiation across AI accelerators necessitates a flexible abstraction layer to handle varying memory organizations. While GPUs employ hierarchical cache structures with L1 and L2 levels, systolic arrays utilize dedicated SRAM scratchpads for weights and feature maps, and other accelerators may implement entirely different memory architectures. These organizational differences extend beyond processing elements themselves to encompass contrasting dataflow patterns, memory access mechanisms, and capacity distributions.

GainSight introduces memory “subpartitions” as a unifying abstraction. Each subpartition represents a distinct memory component, such as cache levels in GPUs, scratchpad buffers in systolic arrays, or specialized storage in custom accelerators. The frontend treats subpartitions as independent entities for lifetime extraction, frequency analysis, and performance projection, enabling consistent evaluation of heterogeneous memory compositions across different architectural paradigms while preserving their unique organizational characteristics.

## 5 ANALYTICAL FRONTEND

GainSight’s analytical frontend transforms raw memory access traces from hardware backends into actionable design insights for heterogeneous memory architectures. As shown in Figure 4, this architecture-agnostic module processes the cycle-accurate traces (5) generated by backends to extract key memory statistics. It then correlates these workload characteristics with memory device retention properties to generate optimal memory compositions and performance projections. The frontend’s modular Python implementation represents a significant portion of GainSight’s codebase and enables systematic evaluation across diverse accelerator architectures and workloads, establishing the foundation for data-driven heterogeneous on-chip memory design.

### 5.1 Memory Device Library

GainSight focuses on StRAM devices to bridge the mismatch between SRAM’s excessive retention and the transient nature of AI workload data. The memory device library (6) in Figure 4 includes 6T SRAM, 3T silicon gain cell RAM (Si-GCRAM), 2T ITO-silicon hybrid gain cell RAM (Hybrid-GCRAM), and 1T1C oxide embedded DRAM (eDRAM), all characterized for the TSMC N5 (5nm) process node.

Memory cell models capture retention times (including write frequency dependence for GCRAM), bit cell area for density projections, and read/write energy per bit for active energy projections. SRAM characteristics derive from TSMC specifications [50, 51], while Si-GCRAM parameters build upon fabricated arrays from Giterman et al. [14] and Pentecost et al. [35], scaled to the 5nm node (N5). Hybrid-GCRAM statistics originate from Liu et al.’s post-layout simulations [27, 28] of 256×256 arrays. Oxide-semiconductor eDRAM parameters derive from Chiang et al. [9], with DRAM-specific operations like precharge amortized into per-bit energy estimates.

This memory device library organization allows straightforward extension to additional memory technologies by only requiring the addition of corresponding performance mockups while maintaining the frontend’s modularity.

### 5.2 Device-Level Memory Access Analysis

The frontend’s analysis pipeline begins by extracting memory statistics (6) from backend-generated traces (5). These statistics include read/write frequencies, unique addresses accessed, and total operation counts.

The module computes data lifetimes (7) as defined in Section 2.4, tracking the temporal interval from each write operation until

the data is overwritten or becomes invalidated. This lifetime distribution is then correlated with the write frequency-dependent retention characteristics of each memory device in the library. Refresh requirements are computed by identifying data objects whose lifetimes exceed the retention limits of the target device, quantifying the number of bit-level refresh operations required to maintain data integrity.

Capacity utilization (8) analyzes unique addresses remaining live simultaneously, scaled by memory block size. This quantifies actual workload memory usage, which may be substantially less than available on-chip memory capacity. Active energy consumption (9) combines weighted read, write, and refresh operations multiplied by device-specific costs, where refreshes are modeled as additional read-then-write operations.

These single-device projections establish baseline comparisons that inform subsequent composition optimization (10) and provide preliminary considerations for heterogeneous array provisioning.

### 5.3 Heterogeneous Memory Composition

The core innovation of GainSight’s frontend lies in computing optimal heterogeneous memory compositions (10) that minimize refresh overhead while maximizing area and energy efficiency. This optimization process begins by analyzing the distribution of data lifetimes across the workload and systematically assigning memory accesses to devices based on a lifetime-retention matching algorithm.

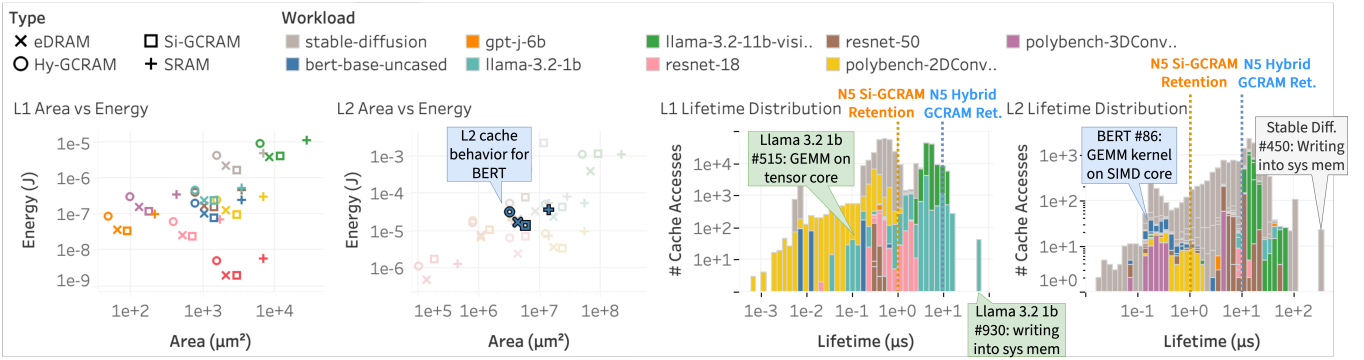
Each memory access is assigned to the device with the shortest retention time that still exceeds the data’s lifetime requirement. This assignment strategy leverages the general trend where Si-GCRAM, Hybrid-GCRAM, and eDRAM offer increasing retention times at the cost of higher active energy consumption. By prioritizing memory devices with minimal necessary retention, the algorithm maximizes the utilization of more energy-efficient short-retention devices while ensuring refresh-free operation.

The assignment process yields the proportion of memory accesses allocated to each device type, which the frontend then correlates with total capacity requirements from (8) to determine the physical area and capacity specifications for each device in the heterogeneous composition. The final optimization generates a comprehensive specification including total array capacity, area footprint, and aggregate energy consumption. This establishes quantitative design guidelines for heterogeneous memory array implementation.

### 5.4 Output Generation and Design Insights

GainSight’s frontend generates three complementary output formats to support comprehensive design analysis, as illustrated in Figure 4: interactive lifetime distribution visualizations (11), quantitative JSON performance reports (12), and optimal memory composition summaries (13).

The Tableau-based visualization framework [40] enables interactive exploration of lifetime distributions across configurations and workloads. Figure 5 demonstrates the interface capabilities, presenting histogram analyses of lifetime characteristics for various memory technologies and workloads. Users can dynamically



**Figure 5: Energy and area projections of L1 and L2 GPU caches implemented with each memory technology, along with the data lifetime distributions of all L1 and L2 accesses across all workloads in Table 5.**

filter results and access detailed workload information through integrated tooltips, facilitating visual comparison and further design insights.

The JSON report provides quantitative metrics essential for systematic design evaluation: refresh requirements quantifying the number of bit-level refresh operations based on write frequency and retention time interactions; active energy consumption encompassing reads, writes, and refreshes; and area requirements derived from unique address access patterns. These metrics are generated both for individual memory devices and for the computed optimal heterogeneous composition, enabling direct quantification of heterogeneous memory benefits over traditional SRAM-only designs.

The composition summary delivers concrete design specifications for the optimal heterogeneous memory configuration, including precise memory array capacity, area allocations, and energy projections. This output directly addresses the design question regarding the quantitative area and performance impacts of heterogeneous on-chip memory design, providing actionable insights for system architects.

In the absence of physically fabricated prototypes for novel on-chip memories, these outputs provide first-order design guidance that facilitates quantitative evaluation of area, energy, and refresh trade-offs across workloads. This capability supports critical design decisions, such as runtime memory provisioning policy development, before physical prototyping becomes available, while abstracting away detailed circuit-level effects that would require additional specialized analysis tools such as SPICE simulations.

## 6 CASE STUDY AND EXPERIMENTS

To illustrate GainSight’s practical application, we conduct two case studies targeting SIMD GPU and systolic array accelerator architectures. These platforms were chosen for their prevalence in AI hardware and their contrasting memory organizations, providing representative evaluations of GainSight’s profiling and analysis capabilities.

We executed a set of workloads from the MLPerf Inference benchmark (v5.0) suite [38] and PolyBench, a polyhedral benchmark of basic ML-related kernels [16, 37], on both backends, as shown in Table 5. For all experiments, we selected input parameters (e.g.,

**Table 5: List of workloads in GainSight’s case studies.**

Name	Test Suite	Description
polybench-2DConv	PolyBench	2D Convolution
polybench-3DConv	PolyBench	3D Convolution
llama-3.2-1b	ML Inference	Meta’s text-based LLM with 1B parameters [43]
llama-3-8b	ML Inference	Meta’s text-based LLM with 8B parameters [43]
llama-3.2-11b-vision	ML Inference	Meta’s LLM with integrated vision adapter for image recognition, total of 11B parameters [43]
resnet-18	ML Inference	CNN for image recognition with 18 layers [20]
resnet-50	ML Inference	CNN for image recognition with 50 layers [20]
bert-base-uncased	ML Inference	“Bidirectional Encoder Representation for Transformers,” uncased text-based LLM with 110M parameters [10]
gpt-j-6b	ML Inference	GPT-like text-based LLM with 6B parameters [48, 49] implemented on the JAX interface
stable-diffusion	ML Inference	Text-to-image transformer model with 3.5B parameters [11]

batch size, input image size, token length) to match common ML inference scenarios and ensure tractable simulation times.

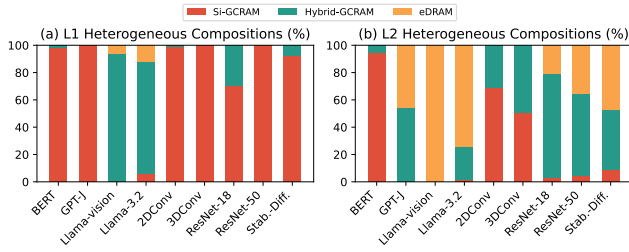
The following sections present detailed experimental results: Section 6.1 examines GPU cache hierarchies, while Section 6.2 explores dataflow-driven memory optimization in systolic arrays. Together, these studies demonstrate GainSight’s ability to inform lifetime-aware memory design across diverse accelerator platforms.

### 6.1 Profiling GPU Workloads

This case study demonstrates GainSight’s lifetime-aware design methodology by evaluating GPU memory hierarchies using our Accel-Sim backend. We analyze data lifetime patterns across L1 and L2 caches for representative AI workloads to evaluate the suitability of different memory devices for these caches and to quantify the benefits of heterogeneous memory compositions.

**6.1.1 Experimental Setup.** The workloads evaluated in this study (Table 5) span transformer-based language models from MLPerf Inference and computer vision benchmarks from PolyBench [16, 37]. They represent the memory-intensive AI inference patterns identified in Section 1 that exhibit data transience characteristics, motivating heterogeneous memory architectures.

Text-based transformer workloads were configured with 7-word input prompts and 20-token generation sequences, while vision workloads processed  $224 \times 224$  pixel images with batch size 1.



**Figure 6: Optimal heterogeneous memory configurations showing capacity proportions of Si-GCRAM, Hybrid-GCRAM, and eDRAM, provisioned based on lifetime profiles for the GPU backend across various workloads.**

These configurations maintain statistical representativeness of real-world memory access patterns while ensuring tractable simulation runtimes through our kernel sampling methodology. Full data and visualizations are available at <https://gainsight.stanford.edu/visualization/index.html> as part of this paper’s artifacts.

**6.1.2 Data Lifetime Characterization.** Figure 5 demonstrates the results of GainSight’s data lifetime analysis and per-device performance evaluation for each workload running on the GPU backend. The scatter plots project area and energy requirements for L1/L2 caches if these caches were implemented with each individual memory device. The histograms display data lifetime distributions for direct correlation with device retention specifications. Vertical reference lines indicate Si-GCRAM (1  $\mu$ s) and Hybrid-GCRAM (10  $\mu$ s) retention times [27]. The ms-scale retention of eDRAM is not shown for conciseness.

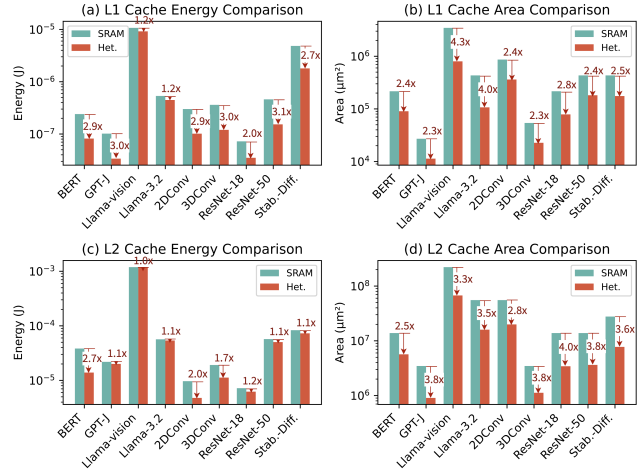
Lifetime analysis reveals substantial fractions of accesses compatible with refresh-free operation on StRAM devices. Specifically, 64.3% of L1 and 18.4% of L2 accesses fall within Si-GCRAM’s 1  $\mu$ s retention, while 97.9% of L1 and 52.0% of L2 accesses fit Hybrid-GCRAM’s 10  $\mu$ s capability [27]. Conversely, significant portions exhibit longer lifetimes (up to 70  $\mu$ s), requiring heterogeneous architectures with longer-retention devices such as eDRAM or SRAM.

Kernel-level analysis reveals that short-lived data predominantly originate from linear algebra operations like GEMM, while longer data lifetimes emerge during memory transfers and nonlinear computations, aligning with Section 1’s architectural motivations.

**Takeaway 6.1.** Data transience is pervasive across the GPU cache hierarchy, with up to 97.9% of L1 accesses and 52.0% of L2 accesses fitting within StRAM retention times, enabling refresh-free operations for non-SRAM, heterogeneous memory architectures.

**6.1.3 Optimal Heterogeneous Memory Configurations.** Leveraging the observed lifetime distributions, GainSight’s frontend generates optimal memory compositions that minimize active energy while ensuring refresh-free operation across Si-GCRAM, Hybrid-GCRAM, and eDRAM technologies. The optimization strategy systematically assigns data to devices with minimal necessary retention times, as detailed in Section 5, prioritizing energy-efficient short-retention memories while guaranteeing data integrity.

Figure 6 illustrates recommended heterogeneous compositions across all workloads in Table 5 and cache levels. Most AI/ML



**Figure 7: Comparison of area and energy savings of heterogeneous L1/L2 caches against monolithic SRAM designs across GPU workloads.**

workloads benefit from Si-GCRAM-dominated L1 caches (>90% of total capacity) with minimal longer-retention allocations. However, transformer models like Llama variants [15] require substantial longer-retention capacity for KV cache storage. L2 caches exhibit more varied lifetime patterns necessitating balanced multi-technology allocations.

Lifetime-optimized configurations achieve substantial improvements over monolithic SRAM designs (Figure 7). Si-GCRAM-dominant L1 caches realize an average 1.89 $\times$  active energy savings, while Hybrid-GCRAM-integrated L2 caches achieve an average of 1.3 $\times$  energy reductions. A consistent memory array area improvement of 3 $\times$  is observed across all workloads compared to baseline SRAM, demonstrating the superior density that a heterogeneous mix of non-SRAM StRAM devices can provide.

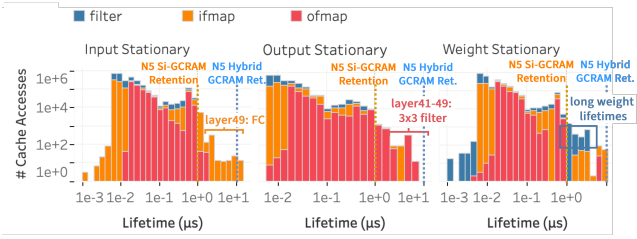
These results validate GainSight’s core methodology that systematic lifetime analysis enables substantial improvements in memory system efficiency by exploiting the mismatch between data transience and SRAM overprovisioning identified in Section 1.

**Takeaway 6.2.** GainSight’s lifetime-aware optimization enables heterogeneous memory architectures that achieve meaningful active energy reductions (up to 3.1 $\times$ ) and area savings (up to 4.3 $\times$ ) by systematically matching workload data lifetimes with optimal memory device retention.

## 6.2 Profiling Workloads on Systolic Arrays

This case study demonstrates GainSight’s versatility across architectures through systematic evaluation of systolic array memory hierarchies using our SCALE-Sim backend. Systolic arrays represent a different paradigm from GPUs, with dedicated scratchpads and deterministic dataflows that facilitate controlled lifetime-retention analysis [22].

**6.2.1 Experimental Configuration.** We evaluated three representative AI workloads, ResNet-50 [20], BERT [10], and Llama-3-1B [43], across PE array configurations ranging from 32  $\times$  32 to 256  $\times$  256



**Figure 8: Data lifetime distributions for ResNet-50 on a  $256 \times 256$  systolic array across three dataflows.**

elements. Each workload’s GEMM operations were analyzed under three canonical dataflows: input stationary (*is*), weight stationary (*ws*), and output stationary (*os*). The accelerator configuration included 4 kB input and weight buffers with an 8 kB output buffer, representing typical edge-oriented systolic array designs.

BERT and Llama used 256-token sequences; ResNet-50 processed  $224 \times 224$  images with single batch execution. These configurations focus on GEMM operations dominating AI inference, while nonlinear operations represent future extensions. For simplicity, we focus on ResNet-50 results in this section, with full experimental datasets available as part of this paper’s artifacts.

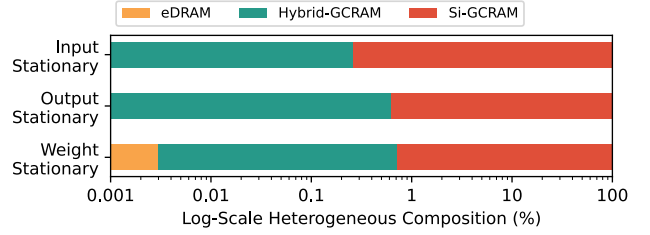
**6.2.2 Dataflow-Dependent Lifetime Patterns.** Figure 8 presents lifetime distributions for ResNet-50 on a  $256 \times 256$  array across three dataflows, demonstrating how mapping decisions influence memory patterns and data lifetimes. Vertical reference lines indicate Si-GCRAM and Hybrid-GCRAM retention times. It can be observed that at least 79.01% of data accesses across input, output, and weight buffers exhibit lifetimes below 1  $\mu$ s, making them suitable for refresh-free storage in 5nm Si-GCRAM.

The histograms show the heterogeneous nature of data lifetimes across buffers and dataflows. Short-lived data emerges from rapid streaming between scratchpads and PE arrays or memory, while long-lived data arises during inactivity periods following PE array saturation in the buffers for the stationary component of the dataflow. This heterogeneity aligns with GPU observations from Section 6.1, suggesting common patterns across accelerator architectures.

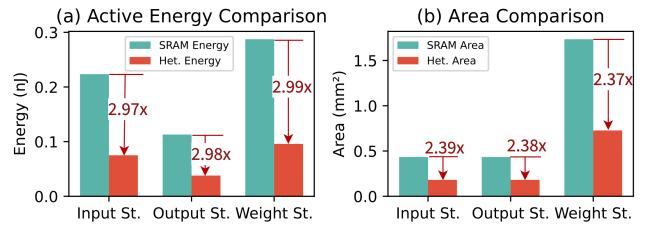
Analysis across dataflows reveals two key insights. First, output feature map (*ofmap*) data consistently exhibits relatively short lifetimes across dataflows, with nearly all data compatible with Hybrid-GCRAM refresh-free operation. This behavior stems from the tight coupling between PE array timing and output feature map generation. Second, dataflow selection primarily affects the maximum lifetime of stationary data structures, as algorithmic stationarity directly correlates with buffer data lifetimes.

**Takeaway 6.3.** Independent of dataflow, *ofmap* data demonstrates consistently short lifetimes suitable for StRAM integration, while *ifmap* and weight data exhibit broader distributions with dataflow-dependent upper bounds.

**6.2.3 Heterogeneous Scratchpad Optimization.** Building upon lifetime characterizations, GainSight generates optimal heterogeneous scratchpad compositions for both stationary and non-stationary data types without refresh overheads (Figure 9). The vast majority



**Figure 9: Optimal heterogeneous memory configurations showing capacity proportions of Si-GCRAM, Hybrid-GCRAM, and eDRAM, provisioned based on lifetime profiles for the systolic array backend on ResNet-50.**



**Figure 10: Comparison of area and energy savings of a heterogeneous scratchpad memory against monolithic SRAM designs on ResNet-50 across three dataflows: Input St(ationary), Output St(ationary), and Weight St(ationary).**

of systolic array scratchpad data across dataflows exhibits short-enough lifetimes compatible with Si-GCRAM, requiring minimal higher-retention Hybrid-GCRAM or eDRAM capacity.

Lifetime-optimized heterogeneous on-chip memory designs achieve substantial improvements over uniform SRAM scratchpads. Figure 10 quantifies  $3\times$  active energy savings and  $2.4\times$  area savings across all dataflows.

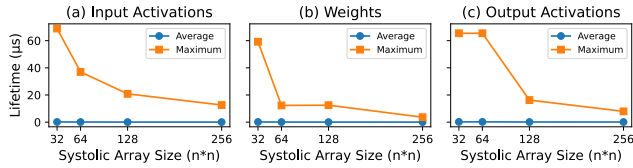
These consistent gains regardless of dataflow reflect the deterministic and predictable nature of systolic array buffer access patterns, where data movement follows well-defined dataflow protocols. These consistent benefits contrast with the more variable improvements observed in GPU experiments, highlighting how architectural determinism in systolic arrays enables more predictable lifetime-driven optimization outcomes compared to the dynamic control flow complexity in SIMD GPU kernels.

**6.2.4 PE Array Scaling Analysis.** An important design consideration in systolic arrays is the size of the processing element (PE) array, which influences data lifetime metrics and scratchpad interactions beyond just area and energy implications.

Figure 11 demonstrates systematic relationships between PE array size and lifetime characteristics.

Larger PE arrays not only incrementally reduce average data lifetimes due to faster data consumption but also narrow the variance of lifetime distributions, where the maximum lifetime of stationary data types decreases significantly.

This systematic reduction in lifetime variance creates opportunities for applying StRAM devices that more aggressively trade off



**Figure 11: Average and maximum data lifetimes across different PE array sizes for ResNet-50 on the SCALE-Sim backend.**

retention time for other benefits such as energy efficiency. This becomes especially beneficial when outlier data lifetimes would otherwise significantly contribute to overall refresh overhead. This observation demonstrates that GainSight’s utility extends beyond informing on-chip memory provisioning to broader architectural design decisions.

*Takeaway 6.4.* Larger systolic arrays narrow the variance of data lifetimes and eliminate long-lived outliers, creating further StRAM integration opportunities.

## 7 DISCUSSION

We have presented GainSight, the first profiling and design exploration framework that correlates dynamic workload lifetime statistics with memory device characteristics to enable optimal heterogeneous memory compositions in AI accelerators. This section discusses GainSight’s broader applicability beyond AI accelerators, examines the future scalability of StRAM technologies, and outlines directions for extending the framework to encompass long-term memory devices.

### 7.1 Data Lifetime Heterogeneity Beyond AI Workloads

GainSight’s lifetime-aware design methodology extends naturally beyond AI accelerators to other domains exhibiting heterogeneous data lifetimes and pervasive short-livedness.

Server workloads exemplify this potential. HTTP buffers and session state demonstrate  $\mu$ s-scale lifetimes ideal for the short-term RAM (StRAM) devices evaluated by GainSight, while cached content suits long-term RAM (LtRAM) technologies in Table 1. Database systems benefit similarly, with transaction logs and query results exhibiting transient patterns favoring StRAM.

Scientific and high-performance computing demonstrates comparable patterns. Simulations generate massive intermediate arrays discarded after convergence – classic StRAM applications – while mesh topology remains static throughout runs. Multimedia pipelines exhibit similar characteristics with brief frame buffers during compression.

These examples underscore the universality of lifetime-aware design principles that GainSight helps establish.

### 7.2 Future of GCRAM Scaling

Given our focus on GCRAM and other StRAM devices, it is important to consider the future of these technologies to ensure they do not fall into the same scaling trap as SRAM. For GCRAM devices, prior work [27] highlights scaling challenges. Decreasing

process nodes increase leakage power and reduce retention time in both Si-GCRAM and Hybrid-GCRAM, even as technologies such as Gate-All-Around (GAA) FETs [50] can reduce the off-current of transistors due to enhanced gate control compared to FinFETs. However, we believe that GCRAM will continue to be a viable option for short-term on-chip memory arrays. Notably, the expected improvement in operating frequency with smaller process nodes mitigates retention requirements, as increasing frequencies allow for more instructions to be completed within a given time frame, reducing real-world lifetimes. Additionally, various circuit-level techniques are available to further enhance retention in advanced technology nodes [19, 52].

## 7.3 Evaluating Long-Term RAM Devices

GainSight currently focuses on on-chip StRAM technologies, specifically GCRAM variants and embedded DRAM. This reflects the significant opportunities for optimizing short-lived data patterns in AI workloads and other data-intensive applications, as demonstrated by our experimental results. While LtRAM devices like RRAM and MRAM offer complementary potential [24, 25], they are excluded because the data transience and high write intensities in this study’s target workloads misalign with LtRAM characteristics. Moreover, effective LtRAM evaluation requires comprehensive endurance modeling that accounts for write frequency, spatial patterns, and temporal clustering over extended operational periods.

Nonetheless, GainSight’s architecture- and device-agnostic infrastructure provides a robust foundation for future extensions to include LtRAM technologies. Subsequent iterations can incorporate LtRAM device models and analytical layers for endurance-aware evaluations. This provides a promising direction for extending heterogeneous memory design across the full spectrum of StRAM and LtRAM technologies.

## 8 CONCLUSION

As SRAM scaling plateaus while AI workloads demand exponentially growing memory capacity, GainSight establishes the first systematic methodology for exploiting the pervasive data transience in these workloads through lifetime-aware heterogeneous on-chip memory design. Our framework bridges the gap between dynamic workload characteristics and emerging short-term memory technologies, transforming accelerator memory design from intuition-driven to profile-guided.

GainSight’s three synergistic contributions – heterogeneous memory composition, unified profiling and evaluation framework, and case studies – provide concrete foundations for the next generation of AI accelerator memory systems. By establishing data lifetime as a first-class design constraint and delivering practical tooling for heterogeneous on-chip memory composition, GainSight enables the architecture community to reimagine on-chip memory as a differentiated resource optimized for data transience.

## ACKNOWLEDGMENTS

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